IN THE CLAIMS

Claims 1-18 **(Cancelled)**

19. **(New)** An information processing apparatus comprising:

an information inputting section operable to input information external to the information processing apparatus;

a first processing section; and

a second processing section,

wherein:

the first processing section is operable to operate in accordance with a first clock having a first frequency,

the second processing section has an operation state, a stop state and a power supply stop state, in the operation state the second processing section operates in accordance with a second clock having a second frequency, in the stop state the second processing section stops operating in accordance with the second clock while the power supply to the second processing section is maintained, in the power supply stop state the power supply to the second processing section is stopped,

the first processing section is operable, when the second processing section is in the stop state, to process the information inputted by the information inputting section and provide to the second processing section, if necessary, an output for initiating the second processing section,

the second processing section in the stop state is operable to make a transition from the stop state to the operation state based on the output from the first processing section,

the second processing section in the power supply stop state is operable to make a transition from the power supply stop state to one of the stop state and the operation state based on an output from the first processing section, and

the second processing section in the operation state is operable to perform a predetermined process based on information output from the first processing section.

20. **(New)** An information processing apparatus comprising:

an Information inputting section operable to input information external to the information processing apparatus;

a first processing section; and

a second processing section,

wherein:

the first processing section is operable to operate in accordance with a first clock having a first frequency,

the second processing section has an operation state, a lower-operation state and a power supply stop state, in the operation state the second processing section operates in accordance with a second clock having a second frequency, in the lower-operation state the second processing section operates in accordance with a clock having a frequency which is lower than the second frequency while the power supply to the second processing section is maintained, in the power supply stop state the power supply to the second processing section is stopped,

the first processing section is operable, when the second processing section is in the lower-operation state, to process the information inputted by the information inputting section and provide to the second processing section, if necessary, an output for initiating the second processing section,

the second processing section in the lower-operation state is operable to make a transition from the lower-operation state to the operation state based on the output from the first processing section,

the second processing section in the power supply stop state is operable to make a transition from the power supply stop state to one of the lower-operation state and the operation state based on an output from the first processing section, and

the second processing section in the operation state is operable to perform a predetermined process based on information output from the first processing section.

21. **(New)** An information processing apparatus according to claim 19, wherein the transition from the stop state to the operation state in the second processing section is made by supplying the second clock to the second processing section in the stop state.

22. **(New)** An information processing apparatus according to claim 19, wherein the second processing section includes a main processing section operable to perform the predetermined process based on the information output from the first processing section, and the main processing section includes a RAM and a register.

23. **(New)** An information processing apparatus according to claim 19, wherein the transition from the power supply stop state to one of the stop state and the operation state in the second processing section is made by supplying the power to the second processing section in the power supply stop state.

24. **(New)** An information processing apparatus according to claim 20, wherein the transition from the lower-operation state to the operation state in the second processing section is made by supplying the second clock to the second processing section in the lower-operation state.

25. **(New)** An information processing apparatus according to claim 20, wherein the second processing section includes a main processing section operable to perform the predetermined process based on the information output from the first processing section, and the main processing section includes a RAM and a register.

26. **(New)** An information processing apparatus according to claim 20, wherein the transition from the power supply stop state to one of lower-operation state and the operation state in the second processing section is made by supplying the power to the second processing section in the power supply stop state.